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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/813,501
Filing Date: March 31, 2004
Appellant(s): BALL ET AL.

Cary Tope-McKay
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/31/06 appealing from the Office action mailed 10/27/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5936440 Asada et al. 8-1999

Millman et al., "Integrated Electronics: Analog and Digital Circuits and Systems", page 568, 1972

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Asada et al. (USP 5936440).

As to claim 1, Asada et al.'s figure 5 shows a method of forming a self-gated transistor (10) comprising: coupling a transistor (841) operable to form a sense signal representative of a current through the self-gated transistor and configuring a first circuit (840, 501, 7) of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor and to enable the transistor responsively to a negative current flow through the transistor. It is noted that col. 6, lines 21-22, teaches that Vr is negative and nearly ground potential. Thus, when Vs is less than Vr, the current flowing through resistor 801 is negative current, and when Vs is greater than Vr, the current flowing through resistor 801 is positive current.

As to claim 2, figure 5 shows that the step of coupling the transistor operable to form the sense signal representative of the current through the self-gated transistor includes forming the transistor having a main transistor portion (10) and a sense transistor (841) as a sensing portion

including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form the sense signal representative of the current through the self-gated transistor.

As to claim 3, figure 5 shows that the step of coupling the main transistor portion to the sensing portion includes coupling a drain of the sense transistor to a drain of the main transistor portion and to the drain of the self-gated transistor and also including coupling a gate of the sense transistor to a gate of the main transistor portion and to the gate of the self-gated transistor.

As to claim 4, figure 5 shows the step of configuring the first circuit of the self-gated transistor to disable the transistor substantially upon the positive current flow through the transistor and to enable the transistor responsively to the negative current flow through the transistor includes coupling a comparator (840, 501, 7) to receive the sense signal wherein the sense signal is positive for the positive current flow and is negative for the negative current flow.

As to claim 5, figure 5 shows that the step of coupling the comparator to receive the sense signal includes coupling a non-inverting input of the comparator to have a negative offset voltage (Vr).

As to claim 6, figure 5 shows that the step of coupling the comparator to receive the sense signal includes coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor.

As to claim 7, figure 5 shows that the step of coupling the comparator to receive the sense signal includes coupling one of a diode or a resistor (801) between a source of a sense transistor and a source of the self-gated transistor.

As to claim 8, figure 5 shows a method of operating a self-gated transistor comprising: providing an MOS transistor having a main transistor portion (10) and a sensing portion (841)

including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion; configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor; configuring the self-gate transistor to conduct a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and configuring the self-gate transistor to detect the second sense signal and responsively enable the self-gated transistor.

As to claim 9, figure 5 shows that the step of configuring-the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes ' configuring the self-gate transistor to steer the second current to flow through a diode (diode that connected to transistor in 841).

As to claim 10, figure 5 shows that the step of configuring the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes configuring the self-gate transistor to steer-the second sense current to f low through a resistor (801).

As to claim 11, figure 5 shows that the step of configuring the self-gate- transistor to detect the first sense signal and responsively disable the self-gated transistor includes ' ' coupling an input of a comparator (840, 501, 7) to receive the first sense signal.

As to claim 12, figure 5 shows a self-gated transistor comprising: a transistor having a main transistor portion (10) and a sensing portion (841) wherein the sensing portion is coupled to the main transistor portion to form a sense signal representative of a current through the self-gated transistor, the main transistor portion having a first gate; and a control circuit (840, 501, 7).

coupled to receive the sense signal and drive the first gate to enable the transistor responsively to a first polarity of the sense signal and to disable the transistor responsively to an opposite polarity of the sense signal.

As to claim 13, figure 5 shows that the control circuit includes a comparator having an inverting input coupled to receive the sense signal.

As to claim 14, figure 5 shows that the comparator has a non-inverting input coupled to a source of the self-gated transistor.

As to claim 15, figure 5 shows that the non-inverting input of the comparator has a negative offset voltage (Vr).

As to claim 16, figure 5 shows that the sensing portion is a portion of the main transistor portion with a source of the sensing portion separated from a source of the main transistor portion and wherein the main transistor portion and the sensing portion have a common drain.

As to claim 17, figure 5 shows that the sensing portion having a source that is separate from a source of the main transistor portion and a protection circuit (840, 501, 7) coupled to the source of the sensing portion.

As to claim 18, figure 5 shows that a source of the main transistor portion is coupled to a source of the self-gated transistor.

As to claim 19, it is inherent for figure 5 to have a voltage regulator (circuit, not shown) coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor (the comparator must be powered in order to operate, the circuit, not shown, that powers the comparator is considered as the voltage regulator).

As to claim 20, figure 5 shows that the self-gated transistor formed in a package having no greater than four leads.

(10) Response to Argument

Appellants argue on page 5, that Asada does not disclose using positive current to disable either one of transistors 10 and 841, and there is no positive current flow through transistors 10/841. The Examiner respectfully disagrees. Col 6, lines 21 and 22, of Asada reference teaches that "the reference voltage Vr is negative and nearly ground potential". Clearly "nearly ground potential" is a potential equal to or very close to ground, e.g. less than 1/10 milli-volt. The output of Asada et al.'s comparator 840 would not change state to turn off transistor 841 immediately after the voltage potential at its negative input terminal increases from a potential below Vr to a potential above Vr because of the comparator input offset voltage. The support for this operation is shown on Millan et al.'s page 568, figure 16-33. Millan et al.'s figure 16-33 shows that the state of the output of a comparator is fully changed when the compared input potential is one milli-volt above or below a reference potential. Therefore, in order for the output of Asada et al.'s comparator to change its state, the voltage at its negative input terminal is at least 1 milli-volt above Vr. Furthermore, transistor 841 would not turn off immediately after the voltage potential at the comparator's negative input terminal increased from a potential below Vr to a potential above Vr because there are delays in Asada et al.'s circuits 7 and 501. Thus, the "less negative voltage" referred to in Appellants' arguments on page 5 that cause transistor 841 to be turned off must be a positive voltage. Since the comparator and the delays of elements 7 and 501 create a voltage offset and Vr is equal to or very close to ground, the voltage at the

negative input terminal of the comparator must be a positive voltage in order to turn off transistor 841. When the negative terminal of the comparator reaches a voltage above ground, the current flowing through transistor 841 is a positive current. Therefore, the Asada reference is seen to anticipate the limitations of claim 1.

Appellants' arguments on pages 7 and 8 are not persuasive for the same reasons above.

Appellants further argue on page 9 that Asada fails to teach a voltage regulator which powers the comparator, and comparator 840 in figure 5 would operate from battery 2 and that a separate voltage regulator is not required to provide the operating voltage to the comparator. The Examiner respectfully disagrees. Asada et al. teaches in col. 2, line 49, that the battery is a vehicle battery. A vehicle battery is a constantly charged voltage source and is regulated by the vehicle engine. Thus, circuit in Asada reference that charges and regulates the battery voltage is seen to meet the claimed voltage regulator.

Appellants further argue that Asada et al. fails to teach that the self-gated transistor formed in a package has no greater than four leads. The Examiner respectfully disagrees. Asada et al.'s figure 5 shows that the number of leads is four, e.g. T5, Vr, 500, and the drain of 841. Applicant further states that figure 1 shows more than five terminals. However, the circuit in figure 5 is being used to anticipate the claimed "self-gated transistor", not the circuit in figure 1.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

Asada et al.'s figure 5 shows all limitations of claims 1-20. Therefore, it is believed that the rejections should be sustained.

Respectfully submitted,

QUAN TRA
PRIMARY EXAMINER

Conferees:

Tim Callahan

Drew Dunn

Quan Tra